UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/717,085 | 11/19/2003 | Ramesh V. Peri | ITL.1059US (P17918) | 7032 |

21906 7590 11/02/2006

TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

| EXAMINER | |
|---|---|
| SCHLIE, PAUL W | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2186 | |

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/717,085
Filing Date: November 19, 2003
Appellant(s): PERI ET AL.



Timothy N. Trop, Reg. No. 28,994
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 7/13/06 appealing from the Office action mailed 3/16/06.

**(1) Real Party in Interest**

The real party of interest is the assignee Intel Corporation.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

U.S. Patent 5,742,790, Kawasaki

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-28 are rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kawasaki (5,742,790).

As per claims 1, 9, 15 and 23, Kawasaki teaches, through acknowledgement of prior art, a processing system and method wherein multiple distinct access requests may be determined to be to a common line of memory by comparing their respective addresses for equality, and thereby enabling their simultaneous (read) access if no otherwise conflicting modifying accesses are simultaneously requested from within said common single line of memory; which may itself be obviously comprised of, in the simplest case, an otherwise conventional single-port memory storing lines of potentially simultaneously accessible data, thereby being effectively equivalent to a multi-port single entry direct mapped cache within which one or more of multiple words may be selected simultaneously through the use of multiple multiplexers associated with each of the ports independently (see abstract lines 1-18, column 1 lines 58-67, column 2 lines 1-7, claim 1 and figures 2-4; and although not cited as the basis of these claim's rejection, please see US Patents cited regarding further reference to common way address detection and utility prior art, including Johnson US 6,629,206 teaching parallel reads in a Harvard Architecture Computer System.)

As per claims 2-8, 10-14, 16-22 and 24-28, being dependant on claim 1, 9, 15, 23, Kawasaki teaches as detailed above, multiple portions of a single line (i.e. sub-lines) may be simultaneously read when corresponding multiple addresses are determined to compare as being equivalent or referencing an equivalently addressed line where neither the architecture of a processor nor the width of the memory or data being

accessed is considered patentably distinguishable as they are not functionally significant to the claimed invention (claims 2-8); and as claims 10-14, 16-22 and 24-28 are considered to correspond to claims 2-8 in other format, they are correspondingly rejected based on the same augments above.

**(10) Response to Argument**

Applicant's arguments filed 7/13/06 have been fully considered but are not persuasive. As although the examiner agrees that a statement made within the examiner's Response to Arguments within the Final Office Action (as cited by the applicant) is not relevant to the rejection of claim 1 (as correspondingly noted within the examiner's response to the applicant's 2/13/06 arguments), and only made in an effort to further clarify that considered to be well known and implicit in that acknowledged as prior art taught by Kawasaki (5,742,790); as the applicant was apparently attempting to argue that as Kawasaki teaches within the "Background of the Invention" (column 1 lines 58-67) that accesses comprising a "write" (i.e. load-store or store-store) may require serialization if referencing a common address, that the reference was not teaching "simultaneous access". Thereby, as claim 1 is specifically limited to "read accesses" (i.e. load-load accesses), the rejection was maintained as the reference clearly teaches that simultaneous access requests not comprising a write (i.e. those comprising only reads/loads) may be performed simultaneously from a multi-port memory, as they would not potentially require serialization to preserve their logical integrity.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Paul W. Schlie

Conferees:

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Matt Kim

Lynne Browne

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100